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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/551,187	04/17/00	ZENG J	SE1443PDA500

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EXAMINER	
TRINH, M	
ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/551,187	Applicant(s) ZENG, JUN	
	Examiner Michael M. Trinh	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *52-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *52-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's preliminary amendment filed on April 17, 2000. Claims 1-51 were canceled. Claims 52-75 have been newly added.

*** Specification page 1, line 1, updating current status of parent application 09/107,721 is respectfully requested.

Claim Rejections - 35 USC § 112

1. Claims 56,57,58,60,67,68,69,71 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 56,57,58,60,67,68,69,71: meaning and scope of "forming same" is unclear and indefinite since it is the "same" of what reference step. It should be deleted.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 52-58,62,65-69,73 are rejected under 35 U.S.C. 102(b) as being anticipated by Pruniaux et al (3,823,352).

Pruniaux teaches a method for forming a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method (at Figs 1-3; col 4, line 1 through col 5) comprising at least the steps of : forming at least one device active region in the semiconductor substrate adjacent a first surface thereof by implantation or diffusion (col 4, lines 1-22); forming at least one recess extending from a second surface of the substrate

(col 5, lines 20-39); forming in the recess at least one lowering body 16 comprising a material having an electrical resistivity lower than that of the semiconductor substrate, wherein the material comprising platinum or platinum silicide; and forming a gold or silver contact layer by electroplating thereon.(col 5, lines 40-47). Re claims 53-54,66, the resistivity lowering body 16 filling the recess (Fig 2C). Re further claim 54, wherein the platinum is a barrier layer lining the recess. Re further claims 56,67, wherein the resistivity lowering body of platinum, gold, silver is inherently having an electrical resistivity less than about 10^{-4} Ohms/cm. Re claims 57,68, wherein as shown in figure 1 a proportion is greater than about 0.4 percent. Re claims 58,69, wherein as shown in figure 2C, the recess extending into the substrate greater than about 25 percent. Re claims 62,73 forming metal oxide semiconductor field effect transistor is mentioned at col 1, lines 5-20.

4. Claims 52-57,59-63,65-68,70-74 are rejected under 35 U.S.C. 102(b) as being anticipated by Obake et al (5,663,096).

Obake teaches a method for forming a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method (at Figs 1-3; col 3, line 52 through col 5) comprising at least the steps of : forming at least one device active region 4/6 in the semiconductor substrate adjacent a first surface thereof (col 3, line 52 through col 3); forming at least one recess extending from a second surface of the substrate (Figs 1,2B); forming in the recess at least one lowering body 26 comprising a material having an electrical resistivity lower than that of the semiconductor substrate (col 5, lines 57 through col 6, line 10), wherein the material comprising Ti-Ni-Au layers, wherein the Au layer is a contact layer. Re claims 53-54,66, the resistivity lowering body 16 filling the recess (Figs 1, 2C). Re further claim 54, wherein the Ti first layer of Ti-Ni-Au layers is a barrier layer lining the recess. Re further claims 56,67, wherein the resistivity lowering body of platinum, gold, silver is inherently having an electrical resistivity less than about 10^{-4} Ohms/cm (Col 6, lines 1-11). Re claims 57,68, wherein as shown in figure 1 a proportion is greater than about 0.4 percent. Re claims 59-61,70-72, wherein as shown, an array of recesses are shown in Figures 1,2C, in a grid pattern, wherein the grid pattern comprising cutting trenches during rotational lapping grinding. Re claims 62,63,73,74, MOSFET and IGBT are mentioned at col 6, lines 47-57.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 63,64,74,75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pruniaux et al (3,823,352).

Pruniaux teaches a method (at Figs 1-3; col 4, line 1 through col 5) for forming a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity as applied above to claims 52-58,62,65-69, and 73.

Pruniaux teaches to form the device as a MOSFET, but lacks to mention to use the device in forming an IGBT (claims 63,74) or a microprocessor (claims 64,75).

However, Obake et al teach (at col 6, lines 47-57) to apply the method in forming a device of MOSFET or IGBT.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method in forming the device of MOSFET or IGBT as combinatively taught by Obake and Pruniaux. This is because of the desirability to form high voltage devices having low ON-resistance. Using these devices for forming a microprocessor, as well known in the semiconductor art, would have been obvious to one of ordinary skill in the semiconductor art because of the desirability to form a computer, wherein the devices are low power consumption.

7. Claims 64,75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obake et al (5,663,096).

Obake teaches a method (at Figs 1-3; col 3, line 52 through col 5) for forming a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, as applied above to claims 52-57,59-63,65-68,70-74.

The references applied above further lack to mention using the device in forming a microprocessor.

It is Official notice that using the device, e.g. MOSFET device having an active region, in forming a microprocessor is well known in the semiconductor art; therefore, it would have been obvious to one of ordinary skill in the art because of the desirability to form a computer with the device having lower power consumption.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Whitehead Jr Carl can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oasc

Michael Trinh
Primary Examiner